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# Design of a frequency reference based on a PVT-independent transmission line delay

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***Abstract*—This paper proposes a novel integrated oscillator topology based on a transmission line. The frequency is extracted from the delay of the transmission line, which is intrinsically independent of temperature and supply variations. The architecture for the oscillator, guidelines for the design of the transmission line as well as the different building blocks are presented. The architecture is based on a phase-locked loop topology. The transmission line used has a 509 ps delay, an area of 2.26 mm$^2$ and a 4.38 dB power loss. The effect of process variations on the transmission line is extensively investigated. A digital driver using CMOS inverters and an analog driver based on an OTA are proposed. Both have a good stability over temperature. The Gilbert cell is proposed as a detector at the output of the transmission line and the corresponding design considerations are shown. Closed loop simulations show fast locking, a variation of 8.3‰ between -10°C and 85°C and a variation of 3.7‰ for $V_{dd} \pm 10\%$.**

## INTRODUCTION

In recent years, a lot of effort is being put in making accurate frequency references without using a crystal [1]–[4]. The elimination of the XTAL oscillator reduces the component count and cost, and has many other benefits [1]. Many proposed oscillators base the frequency on properties that depend on temperature such as mobility or resistivity, and thus involve complicated compensation schemes [3], [4]. We propose a design in 130 nm based on the delay of a transmission line. The delay is determined by the propagation speed, a constant over PVT variations.

The paper is structured in five sections. Section I discusses the architecture that generates an oscillation based on the delay. Section II comments on the different trade-offs that arise when designing a transmission line as a delay block. Section III elaborates the driver for the transmission line and section IV proposes a phase detection scheme. Section V discusses the results of the simulations and the overall performance of the oscillator.

## I. ARCHITECTURE

We have developed an architecture that eliminates the influence of parasitics in order to obtain an accurate oscillator. Figure 1 shows the proposed architecture. It is based on the structure of a phase-locked loop where a voltage-controlled oscillator (VCO) generates an output signal. This signal is buffered and sent through a transmission line. The transmission line has a constant delay and introduces a phase shift depending on the frequency. Subsequently, the output of the transmission line is used as an input for the phase detector. The other input of the detector is equal to the input of the transmission line. A standard phase detector will force the oscillator to change the frequency until the phase shift across the transmission line is 180°, thereby fixing the frequency at $f = 1/2\tau_{delay}$. The oscillator runs at 500 MHz.

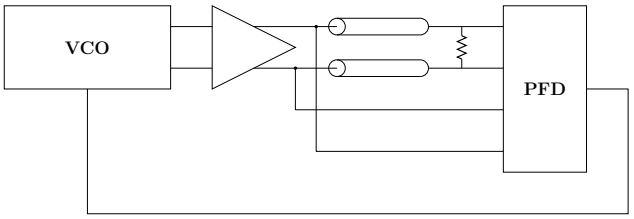
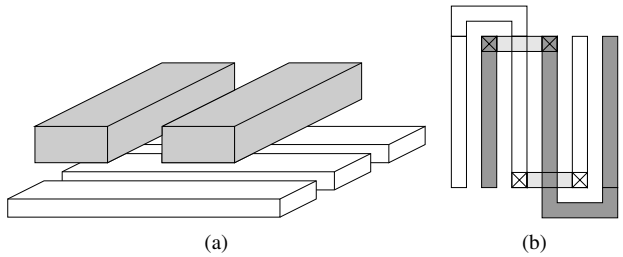



Fig. 1. Architecture of the oscillator. A differential voltage controlled oscillator generates the signal. It is buffered by the line driver and sent through the transmission line. The phase frequency detector (PFD) compares the output of the transmission line and the inverted input of the transmission line and steers the VCO.

The architecture has three important consequences. To start with, all signals at the oscillator frequency are differential. This allows for more accuracy in the line driver and the phase detector, and results in better operation of the transmission line. Secondly, the VCO topology can be chosen freely, which allows for a wide variety of oscillators, and the oscillator can thus be chosen according to the demands for area, power consumption, spectral purity, etc. Finally, the frequency is only determined by the delay of the transmission line.

Frequency variations are caused by only four elements. First of all, it can be due to temperature- and process-induced variations on the waveform produced by the driver, resulting in a different distortion in the transmission line and a slightly different delay. A second origin of inaccuracy is the termination of the transmission line. In order to avoid reflections, a load has to be attached at the end of the transmission line. The load may depend on temperature and process variations and thus influences the waveform at the output of the transmission line. A third element is the phase detector. If the phase difference $\theta$ for which the phase detector gives a zero output shifts depending on temperature or process, it will have a direct influence on the lock frequency. Finally, the charge pump (which is part of the phase detector) may exhibit some asymmetry due to mismatch, again changing the phase where locking occurs and thus influencing the frequency.



(a) (b)

Fig. 2. (a) Structure of a slow-wave transmission line. The conductors are gray. (b) Folding the transmission line. Conductor 1 is white, conductor 2 is dark gray, and the metal layer below the main layer is gray.

## II. Transmission line design

The transmission line has a large impact on the accuracy, the area and the power consumption and therefore should be designed carefully. The transmission line can be implemented as a regular differential transmission line or as a *slow-wave* transmission line [5], [6]. Slow-wave transmission lines are typically made by putting small transversal strips under a pair of wires. The strips are electrically floating, as seen in figure 2a. The strips introduce increased capacitance per meter between the wires, while the inductance per meter remains approximately the same. As a consequence, the simulated group delay of the transmission line [7] increases spectacularly, by a factor between 1.5 and 4.5. The use of slow-wave transmission lines can thus save a lot of area.

### A. Design parameters

The most important characteristics of transmission lines are group velocity, characteristic impedance and losses. Lower metal layers introduce more losses. Therefore using the highest metal layer gives better results. Increasing the width of the conductor reduces losses, but also decreases the impedance of the line. Moreover, the line takes more area per unit length. Changing the gap between the conductors mainly influences the characteristic impedance of the line and has little other influence.

In traditional on-chip transmission lines, group velocities around $10^8$ km/s can be expected. For a delay of 500 ps, a transmission line of around 50 mm would be required, which can be a challenge from an economical point of view. Using transmission lines with slow-wave effect therefore is highly beneficial, as they have an area reduction of between 33% and 78% for the same delay.

### B. Process variations

The delay of the transmission line depends on some process parameters, such as the oxide thickness and metal thickness, which can change from wafer to wafer due to process variations. Assuming that the variation on the thickness of each layer equals $\pm 15\%$ of the thickness of the thinnest layer, a significant variation on the delay can be observed. For a standard transmission line of $100\mu m$ long, a variation of 2.68% on the delay can be observed. For a slow-wave transmission line with a 1.5 times higher delay, the total variation on the delay increases to 6.61%. The dominant reason of this increase is the variation on the vertical capacity to the strips, because it is inversely proportional to the oxide thickness. An increased vertical capacity also introduces increased slow-wave effect; therefore the sensitivity of the delay to the process variations increases with the slow-wave effect. A trade-off emerges: a smaller area due to the slow-wave effect can be traded for a reduced variation over the process. In the end, we therefore chose to use a transmission line without slow-wave effect.

| | |
|---|---|
| Length | 55.5 mm |
| Delay | 509.0 ps |
| Characteristic Impedance | 129 Ω |
| Power losses | 4.38 dB |
| Area | 2.264 $mm^2$ |
| Process variation on delay | 4.36 % |

TABLE I. Properties of the full non slow-wave transmission line at the design frequency (500 MHz)

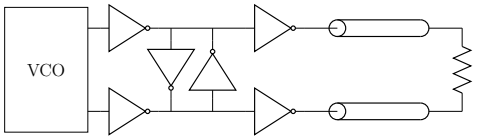



Fig. 3. The proposed digital driver. It contains two inverter chains, which are synchronised by a small inverter pair.

### C. Designing a full line

As the required length of 50 mm is far longer than the length of a chip, the transmission line is folded. Figure 2b shows the used technique to fold a line. Important properties of the technique are symmetry and constant alternation of the two conductors in the transversal direction. The gap between all conductors is the same.

A complete line with a length of 55.5 mm has been simulated with a gap between the conductors $G = 10\ \mu m$ and a conductor width $C = 10\ \mu m$. The results are summarized in table I. It is possible to reduce the area by reducing $G$ and $C$, introducing however more losses.

## III. Line drivers

As the characteristic impedance of a transmission line is rather low, providing sufficient current can be quite difficult: a powerful line driver is required. As noted in part I, the drivers must be differential. The line can be driven in a digital or analog way. The choice is very important as the transmission line behaves differently for sinewaves compared to block pulses and it influences the detector design.

### A. Digital driver

A digital driver generally consists of two inverter chains. By using sufficiently large transistors for the last stage, a large current can easily be supplied. The voltage swing is therefore large (nearly rail-to-rail) and the driver generates steep edges. In order to cope with asymmetries in the inverter chains, a small cross-coupled inverter pair can be inserted in front of the last stage. The inverter pair functions as a small memory cell, but is easily overpowered and synchronises the two chains. In figure 3 the schematic of the proposed digital driver is shown.

| | Digital | Analog |
|---|---|---|
| Voltage swing (V) | 1.08 | 0.30 |
| Temperature dependence (ppm/°C) | 5.6 | 56 |
| Power consumption (mW) | 11.2 | 7.2 |

TABLE II. PROPERTIES OF THE PROPOSED DRIVERS

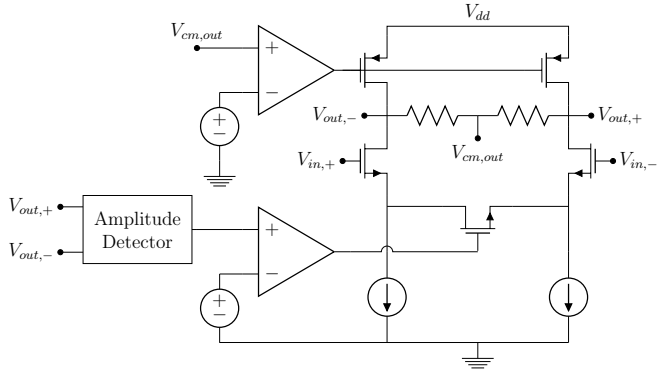



Fig. 4. The proposed analog driver. It contains common-mode feedback on the load transistors and source degeneration to regulate the output amplitude.

### B. Analog driver

The proposed analog driver is based on a single-stage operational transconductance amplifier (OTA), as depicted in figure 4. The driver is fully differential. A common-mode feedback using an additional small OTA is needed to keep the DC output voltage node constant. Additionally, an amplitude detector is added to ensure that the waveform at the output is as constant as possible over process and temperature. The gain of the stage is controlled by source degeneration, and the level of degeneration is set by a small OTA so that the output amplitude is fixed.

In table II the most important properties of both drivers are summarized. Because of the high level of symmetry and the process independence and lower power, the analog implementation is preferred in the end.

## IV. THE PHASE DETECTOR

Several circuits can be used as a phase detector [8], [9]. We used the Gilbert cell [10], an analog multiplier. A simple schematic is given in figure 5. By filtering out the DC component, the Gilbert cell effectively functions as a phase detector with a zero output for 90° input phase difference. The Gilbert cell can be used to detect both analog and digital signals and is inherently differential.

### A. Termination of the line

In order to prevent reflections at the end of the transmission line, an appropriate load should be connected to the end of the line. In case of an analog driver, the load is a resistor with the magnitude of the characteristic impedance. For the digital case, a trade-off is observed: a larger resistor will increase the swing at the output of the line due to reflection [7], but it will also increase temperature dependence. As a compromise, a resistor with two times the characteristic impedance was chosen. The parasitic capacitance is caused by the input of the phase detector and should be kept as small as possible, as

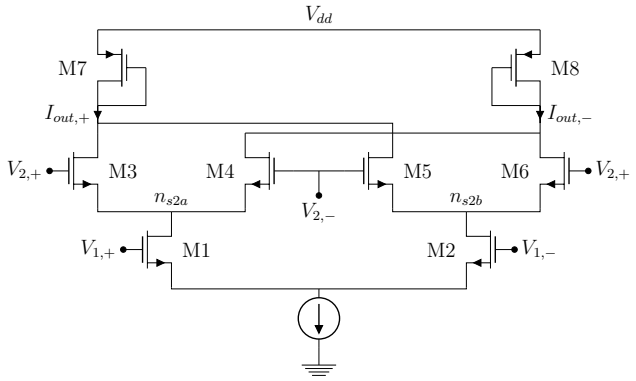



Fig. 5. Gilbert cell used as a phase detector [10]

it reduces the swing and decreases the slopes at the output of the transmission line.

### B. Inaccuracy in the Gilbert cell

There are two main sources of inaccuracy in the Gilbert cell. First, there is the mismatch in the differential pairs, introducing an offset voltage at the input. Switching does not occur exactly when the signals cross but when they are $V_{offset}$ apart, and thus it introduces a delay depending on the input slope. The mismatch can be limited by increasing the size of the input transistors.

Secondly, parasitic capacitances at nodes $n_{s2a}$ and $n_{s2b}$ in figure 5 introduce inaccuracy. When the current through $M_1$ increases, the combined current through $M_3$ and $M_4$ increases as well. This happens by lowering their virtual ground voltage at $n_{s2a}$, which requires some discharge of the parasitic capacitor. This introduces some extra delay and the detector will generate a zero output for a phase larger than $90°$. Since the capacitance depends on temperature and process, the delay of the zero output phase will be temperature dependent. The main origin of the capacitance is the $C_{GS}$ of transistors $M_3$ and $M_4$, which can be decreased using small transistors. This conflicts with the above requirement.

### C. Digital and analog implementation

A practical implementation has to cope with a problem introduced by the architecture. Since the signal at the end of the transmission line is just a delayed and reduced version of the input signal, the DC value for both is the same. As the proposed topology stacks two transistors, it is difficult to design them with both the same DC gate voltage.

In an implementation with large signals at the inputs, hereafter called digital implementation, transistors $M_1$ and $M_2$ are used as digital, switching transistors. They are designed wide to avoid a large voltage drop. The DC gate value for transistors $M_3$, $M_4$, $M_5$ and $M_6$ is $V_{dd}/2$, which is rather low considering the limited voltage headroom.

In an analog implementation the problem is even more prominent. In order to keep the lower transistors in saturation, the overdrive voltage $V_{GS} - V_T$ of the upper transistors is limited by $V_{T,M_{12}} - V_{T,M_{3456}}$. This can be increased by using a transistor with a higher threshold voltage for the

| | Digital | Analog |
|---|---|---|
| DC input voltage (V) | 0.6 | 0.9 |
| Temperature dependence (ppm/°C) | 68 | 26 |
| Process variation ($\sigma$) | 0.35% | 9.6% |

TABLE III. PROPERTIES OF THE DESIGNED GILBERT CELLS

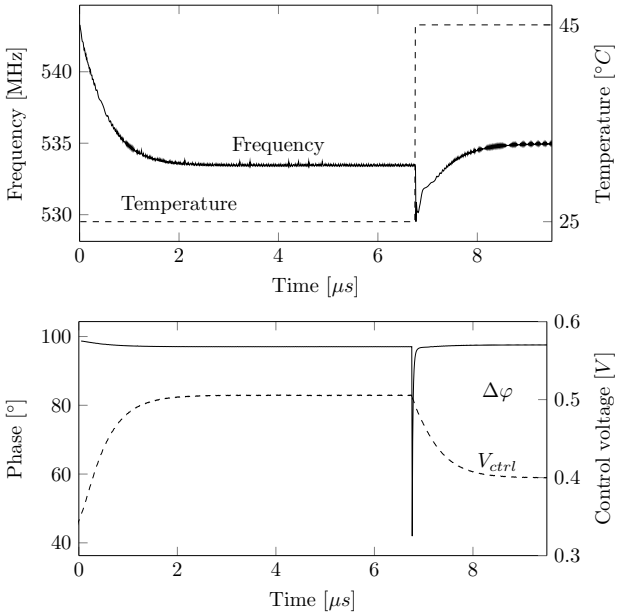



Fig. 6. System response to booting and to applying a temperature step.

lower transistor, which is either provided by the technology or generated by choosing the length according to the $L$ - $V_T$ relation. The analog implementation is more sensitive to process variations, because the transition slope is smaller. The results of the prototype design of the Gilbert cell are listed in table III.

## V. COMPLETE SYSTEM

To prove the feasibility of the topology, closed-loop simulations have been performed. For a prototype design with an analog driver, the system response to booting and a temperature step is plotted in figure 6. It is clear that a fast and accurate locking occurs. The frequency is plotted as a function of the temperature in figure 7. The total variation between $-10°$C and $85°$C is 8.3‰ and the worst-case sensitivity is 226 pm/°C. Variations on the supply voltage of $\pm 10\%$ cause a variation of 3.7‰ on the frequency.

## VI. CONCLUSION

An oscillator architecture based on a traditonal PLL with a transmission line is presented. By adapting the topology, it is possible to make a frequency reference that only depends on the delay of a transmission line, which is intrinsically independent of temperature and supply variations. Different techniques to decrease the area such as slow-wave transmission lines were investigated. From this, a standard differential transmission line in the upper metal layer is the most process independent solution. We also proposed two line drivers. The digital driver is based on two inverter chains, which are synchronised by a clock latch. The analog driver is based on the fully differential

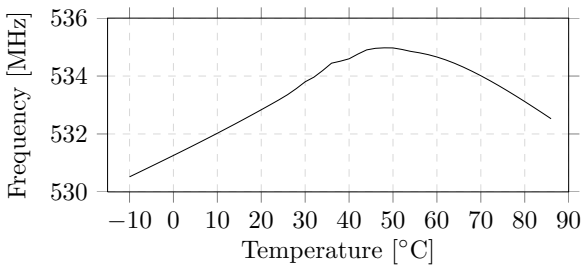



Fig. 7. The frequency of the oscillator as a function of the temperature for a prototype analog driver.

OTA with source degeneration. The output DC levels and the output amplitudes are controlled by feedback loops, which makes it ultimately more stable. Finally, the Gilbert cell is proposed as a phase detector. It is intrinsically differential and promises an excellent performance due to its symmetry. It can be used to detect signals from both a digital and an analog driver. The origins of inaccuracies in the Gilbert cell are mismatch and parasitic capacitances. The complete system has a variation of 8.3‰ over the temperature and supply variation of 3.7‰.

## ACKNOWLEDGMENT

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